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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/477,790	12/31/1999	GEOFF BARRETT	S1022/8363	9742

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EXAMINER	
DAY, HERNG DER	
ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,790	BARRETT, GEOFF	
	Examiner	Art Unit	
	Herng-der Day	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/028,415* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-21 have been examined and claims 1-21 have been rejected.

Priority

2. Acknowledgment is made of a claim for domestic continuation-in-part priority of U.S. Patent Application Serial No. 09/028,415, filed on February 24, 1998, and a foreign priority under 35 U.S.C. 119(a)-(d) filed in United Kingdom on September 3, 1997.

Drawings

3. The Draftsperson has objected to the drawings; see the copy of Form PTO 948 for an explanation. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

4-1. As described in lines 7-9 of page 8, "to provide a new set of states which represent the pre-image of the reverse system thus the post-image of the second system". It is unclear what the second system is referred to.

5. The incorporation of essential material in the specification by reference to a foreign application, as shown in page 5, is improper. Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

Claim Objections

6. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends on a dependent claim, should not be separated by any claim which does not also depend on said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

For example, claim 17 depends on the dependent claim 15, should not be separated by claim 16, which does not also depend on dependent claim 15.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

8-1. For example, all the equations as described in the last line of page 5 and in lines 3-4 and 7 of page 6 are obviously incorrect. These equations contain either unpaired parenthesis or even without equal sign. It is unclear for one skilled in the art how to make and/or use the invention without undue experiment because even the exemplary procedure is not enabled.

8-2. As described in lines 8-13 of page 2, "The formation of the reverse model may include transforming a transition function of the system into a constraint on the reverse model, and applying a parameterization of the constraint to all transitions of the reverse model". However, the individual transition determines the relationship between the individual state, for example, the transition from state S1 to state S2 is T12 as explained in page 4, fifth paragraph. Therefore, all transitions of the reverse model have already characterized the reverse model completely. Any modification of any transition will eventually form a different reverse model. Accordingly, it is unclear for one skilled in the art why and how to apply a parameterization of the constraint to all transitions of the reverse model without eventually altering the reverse model.

8-3. As described in the first paragraph of page 3, "The logical device is constructed and arranged to substitute the state variables of the reverse model by transition functions of the reverse model to provide a new set of states representing the pre-image of the reverse model, and thus provide the post-image in the system". However, for any finite state machine, transition

functions may include inputs but state variables may not include inputs. Accordingly, unless it is an autonomous system, it is unclear for one skilled in the art how to avoid introducing inputs into state variables when substitute the state variables by transition functions.

8-4. Claims 1 and 5-7 recite the limitation "control system" in each claim and claims 2-4 and 8-21 recite the limitation "electronic circuit" in each claim. However, in the specification, only bits representative of states and transition functions are used and the parameterization technique is implemented by Boolean operations. Specifically, in lines 4-5 of page 5, Applicant admits, "The invention accordingly provides a method and apparatus for synthesizing a reverse model of a finite state machine". Accordingly, it is unclear for one skilled in the art how to make and/or use the invention without undue experiment when the "control system" or "electronic circuit" cannot be represented by a finite state machine.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 13 and 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10-1. Claim 13 recite the limitation "said reverse system" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "said reverse system" as described in claim 13 refers to "said reverse model".

10-2. Claim 15 recite the limitation "said reverse system" in line 8 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim

examination, the Examiner will presume that "said reverse system" as described in claim 15 refers to "said reverse model".

10-3. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 5-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,031,983. Although the conflicting claims are not identical, they are not patentably distinct from each other because by applying the patented post image techniques and device for synthesizing a reverse model of a system will not only meet the limitations of claims 5-21 but also have the benefit of providing an efficient formal verification method for a finite state sequential machine.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the patented post image techniques and device for synthesizing a

reverse model of a system because a formal verification for a finite state sequential machine can be efficiently accomplished.

Claim Interpretation

13. Claims 1 and 5-7 recite the limitation "control system" in each claim. However, only finite state machine has been supported in the specification, as detailed in section **8-4** above. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner will interpret the "control system" as a "finite state machine".

14. Claims 2-4 and 8-21 recite the limitation "electronic circuit" in each claim. However, only finite state machine has been supported in the specification, as detailed in section **8-4** above. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner will interpret the "electronic circuit" as a "finite state machine" and inherently may include logic circuit and microprocessor.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Vai et al., "Qualitatively Modeling Heterojunction Bipolar Transistors for Optimization: a Network

Approach", Proceedings, IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, August 1993, pages 219-227 (IDS Cite No. C8, paper # 5).

16-1. Regarding claim 1, Vai et al. disclose a method of synthesizing a reverse model of a control system comprising:

transforming a transition function of the control system into a constraint on the reverse model (Constraints, Figure 4); and

applying a parameterization of said constraint to all transitions of the reverse model (Mapping Algorithm, Figure 4).

16-2. Regarding claim 2, Vai et al. disclose a method of synthesizing a reverse model of an electronic circuit (heterojunction bipolar transistors, abstract), the method comprising:

transforming a transition function of said electronic circuit into a constraint on the reverse model (Constraints, Figure 4); and

applying a parameterization of said constraint to all transitions of the reverse model (Mapping Algorithm, Figure 4).

16-3. Regarding claims 3 and 4, Vai et al. further disclose said electronic circuit includes a logic circuits or a microprocessor (finite state machine inherently includes logic circuit and microprocessor, as detailed in section **14** above).

17. Claims 5-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Wu et al., "A Massively Parallel Reverse Modeling Approach for Semiconductor Devices and Circuits", Proceedings, 1997 IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, August 1997, pages 201-209 (IDS Cite No. C9, paper # 5).

17-1. Regarding claim 5, Wu et al. disclose a method of calculating the post-image in a control system, the method comprising:

forming a reverse model of said control system (Reverse Modeling, page 207, section V); and

calculating the pre-image in said reverse model, wherein the pre-image in said reverse model is equivalent to the post-image in said control system (Desired Output Characteristics, Fig. 5).

17-2. Regarding claim 6, Wu et al. further disclose identifying from a characterization of a model of said control system, transitions of said control system and reversing said transitions to form potential transitions of a reverse model (backpropagation learning rule, page 207, last paragraph).

17-3. Regarding claim 7, Wu et al. further disclose extracting from a characterization of a model of said control system, transition functions of said control system (leaning formula, page 207, last paragraph).

17-4. Regarding claim 8, Wu et al. disclose a method of calculating the post-image in an electronic circuit (RF amplifier, Fig. 3), the method comprising:

forming a reverse model of said electronic circuit (Reverse Modeling, page 207, section V); and

calculating the pre-image in said reverse model, wherein the pre-image in said reverse model is equivalent to the post-image in said electronic circuit (Desired Output Characteristics, Fig. 5).

17-5. Regarding claims 9 and 10, Wu et al. further disclose said electronic circuit includes a logic circuits or a microprocessor (finite state machine inherently includes logic circuit and microprocessor, as detailed in section **14** above).

17-6. Regarding claim 11, Wu et al. further disclose identifying from a characterization of a model of said electronic circuit, transitions of said electronic circuit and reversing said transitions to form potential transitions of a reverse model (backpropagation learning rule, page 207, last paragraph).

17-7. Regarding claim 12, Wu et al. further disclose extracting from a characterization of a model of said electronic circuit, transition functions of said electronic circuit (leaning formula, page 207, last paragraph).

17-8. Regarding claim 13, Wu et al. disclose a device for synthesizing a reverse model of an electronic circuit, the device comprising:

a first store storing bits representative of transition functions of said electronic circuit (input-output patterns, page 204, first paragraph);

a second store storing bits representative of an estimate of transition functions of said reverse model (mapping functions, page 204, first paragraph); and

a processing system comprising

a logical device for transforming said transition functions of said electronic circuit into constraints on said reverse model (hidden layers, page 204, first paragraph); and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of said reverse model to form transition functions of said reverse model (backpropagation algorithm, page 205, second paragraph).

17-9. Regarding claim 14, Wu et al. disclose a device for calculating the post-image in an electronic circuit comprising:

a third store storing bits representative of transition functions of a reverse model of said electronic circuit (input-output patterns, page 204, first paragraph);

a fourth store storing bits representative of a set of states of said electronic circuit (neuron, page 203, second paragraph); and

a forming device substituting the state variables of the reverse model by the transition functions of the reverse model to provide a new set of states representing the pre-image of said reverse model, and thus provide the post-image in said electronic circuit (backpropagation learning process, page 204, first paragraph).

17-10. Regarding claim 15, Wu et al. further disclose comprising a first store storing bits representative of transition functions of said electronic circuit;

a second store storing bits representative of an estimate of transition functions of said reverse model (mapping functions, page 204, first paragraph);

a logical device for transforming said transition functions of said electronic circuit into constraints on said reverse models (hidden layers, page 204, first paragraph); and

a parameterization processor for applying a parameterization of said constraints to said estimate of transition functions of the reverse system to form transition functions of said reverse model (backpropagation algorithm, page 205, second paragraph).

17-11. Regarding claim 16, Wu et al. further disclose said estimate of transition functions of said reverse model comprises previous state variables of said electronic circuit (another set of outputs, page 205, second paragraph).

17-12. Regarding claim 17, Wu et al. further disclose said estimate of transition functions of said reverse model comprises previous state variables of said electronic circuit (another set of outputs, page 205, second paragraph).

17-13. Regarding claims 18 and 19, Wu et al. further disclose said electronic circuit includes a logic circuit or a microprocessor (finite state machine inherently includes logic circuit and microprocessor, as detailed in section **14** above).

17-14. Regarding claims 20 and 21, Wu et al. further disclose said electronic circuit includes a logic circuit or a microprocessor (finite state machine inherently includes logic circuit and microprocessor, as detailed in section **14** above).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reference to Filkorn, U.S. Patent 5,491,639 issued February 13, 1996, is cited as disclosing a procedure for verifying data-processing systems.

Reference to Pixley et al., "Exact Calculation of Synchronizing Sequences Based on Binary Decision Diagrams", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, August 1994, pages 1024-1034, is cited as disclosing calculation of synchronizing sequences.

Reference to Cabodi et al., "Symbolic Exploration of Large Circuits with Enhanced Forward / Backward Traversals", Proceedings of the Conference on European Design

Automation Conference, 1994, pages 22-27, is cited as expressing enhanced forward / backward traversals.

Reference to Iwashita et al., "CTL Model Checking Based on Forward State Traversal", Proceedings of the 1996 IEEE/ACM International Conference on Computer-Aided Design, November 1996, pages 82-87, is cited as expressing forward state traversal.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
June 30, 2003